C8051F338

25 MIPS, 16 kB Flash, 10-Bit ADC, 24-pin Mixed-Signal MCU

Analog Peripherals

10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 16 external inputs; programmable as single-ended or differential
- Reference from internal V_{REF}, V_{DD}, or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor

10-bit DAC (Current Mode)

Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Supply Voltage: 2.7 to 3.6 V

Temperature Range: –40 to +85 °C

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory

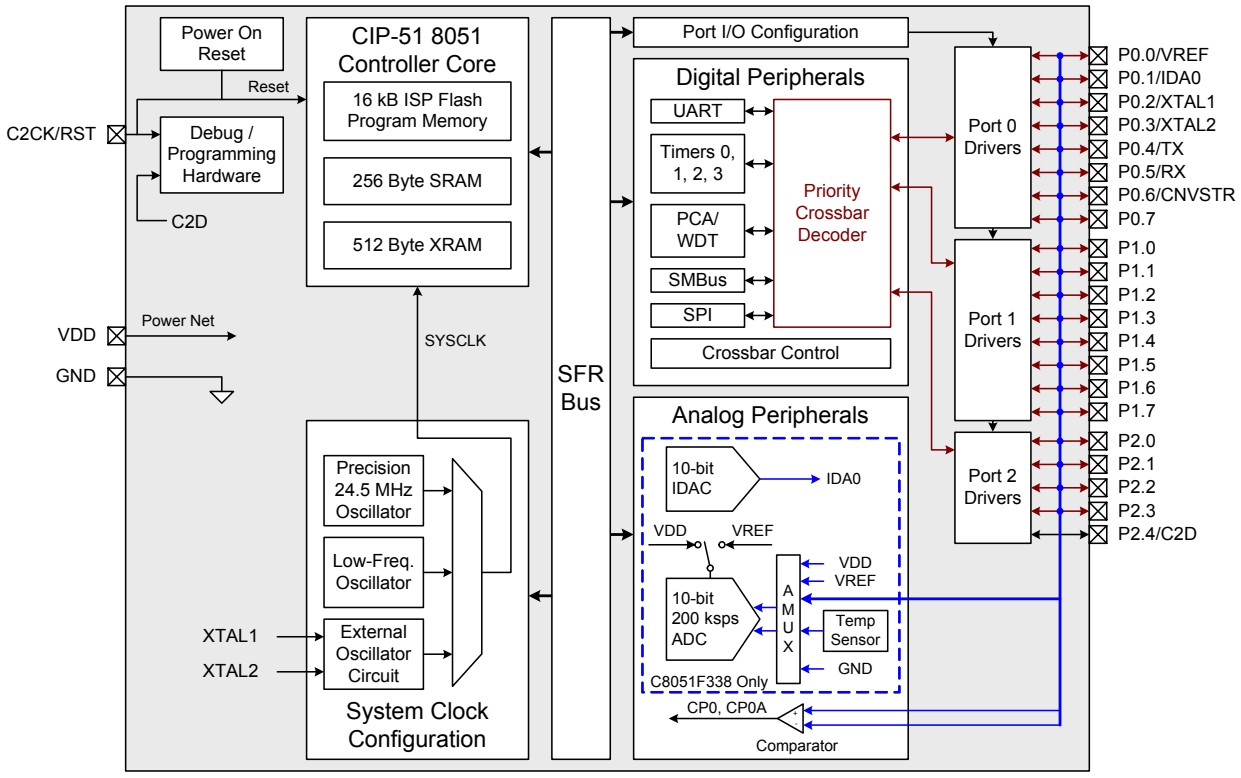
- 768 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

Digital Peripherals

- 21 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I^2C™ compatible), SPI™, and crystaless-UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Timer with real-time clock mode
- Clock sources
- Two internal oscillators:
  - Precision 24.5 MHz, 2% accuracy over V_{DD} and temperature
  - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly
- Suspend mode for maximum power savings with fast wake-up (<1 us)

Package

- 24-pin QFN



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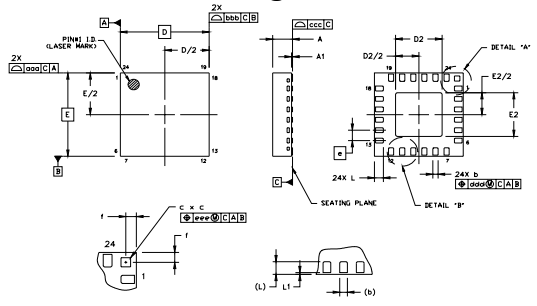
Selected Electrical Specifications

(T_A = –40 to +85 C°, V_{DD} = 2.7 V unless otherwise specified)

	Conditions	Min	Typ	Max	Units
Global Characteristics					
Supply Voltage			—	3.6	V
Supply Current with CPU Active	Clock = 25 MHz	—	TBD	—	mA
	Clock = 1 MHz	—	TBD	—	mA
	Clock = 80 kHz; V_{DD} monitor disabled	—	TBD	—	µA
	Clock = 32 kHz; V_{DD} monitor disabled	—	TBD	—	µA
Supply Current (shutdown)	Oscillator off; V_{DD} monitor disabled	—	TBD	—	µA
Clock Frequency Range			—	25	MHz
Internal Oscillators					
Frequency (OSC0)			24.5	25.0	MHz
Frequency (OSC1)			80	—	kHz
A/D Converter					
Resolution					bits
Integral Nonlinearity			±½	TBD	LSB
Differential Nonlinearity	Guaranteed monotonic	—	±½	TBD	LSB
Signal-to-Noise Plus Distortion			55.5	—	dB
Throughput Rate			—	200	ksps
Input Voltage Range			—	V_{REF}	V
D/A Converter					
Resolution					bits
Integral Nonlinearity			±½	—	LSB
Differential Nonlinearity	Guaranteed monotonic	—	±½	TBD	LSB
Output Settling Time			5	—	µs
Comparator					
Response Time Mode0	(CP+) – (CP–) = 100 mV	—	TBD	—	µs
Current Consumption Mode0			TBD	—	µA
Response Time Mode1	(CP+) – (CP–) = 100 mV	—	TBD	—	µs
Current Consumption Mode1			TBD	—	µA
Response Time Mode2	(CP+) – (CP–) = 100 mV	—	TBD	—	µs
Current Consumption Mode2			TBD	—	µA
Response Time Mode3	(CP+) – (CP–) = 100 mV	—	TBD	—	µs
Current Consumption Mode3			TBD	—	µA

QFN-24 Package Information



Dimension	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.19	0.24	0.29
D		4.00 BSC.	
D2	2.00	2.10	2.20
e		0.50 BSC.	
f		0.27 BSC	
E		4.00 BSC.	

Dimension	Millimeters		
	Min	Nom	Max
E2	2.00	2.10	2.20
L	0.30	0.40	0.50
L1	0.03	0.05	0.08
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

C8051F338DK Development Kit

Small Form Factor

08.13.2007